COMM\_TO IP SPEC

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## Introduction

Count the interval time between 2 successive FRAME\_DONE in active mode. If the time is longer than a threshold, output SET\_SCTO or SET\_LCTO.

## Feature

Key features of the COMM\_TO module is:

Count the interval time between 2 successive FRAME\_DONE in active mode.

Timout counters support being programmed from 100ms to 1h with 8 steps, accuracy 5%.

## Register Definition

### Register Map

Table 1 COMM\_TO Register Map

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Name** | **Add** | **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** | **default** |
| COMM\_TO | 0x0003 | LCTO\_SEL<1:0> | | PROG\_LCTO<2:0> | | | PROG\_SCTO<2:0> | | | 0xA3 |

## Functional Details

### Block Diagram

The following diagram shows the COMM\_TO inputs and outputs.



Figure1 COMM\_TO diagram

### Module input/output list

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Name | Dir | Width | Discirption | duration |
| D2A\_LONG\_TO | O | 1 | Scan-muxed long timeout | Level(CLK\_REG domain) |
| SET\_SCTO | O | 1 | Short timeout | Level(CLK\_REG domain) |
| SET\_LCTO | O | 1 | Long timeout | Level(CLK\_REG domain) |
| CLK\_REG\_SC | I | 1 | Scan-mux result of 8MHz clock from CLK\_32M | 8MHz |
| resetb\_CLK | I | 1 | Asynchronous reset signal(synchronously released) | Level(CLK\_32M domain) |
| pulse\_1M | I | 1 | Pulse with 1us period with 12.5%duty | 1 CLK\_REG |
| resetb\_CLK | I | 1 | Short timeout | Level(CLK\_REG domain) |
| rstb\_32M\_ok\_and\_sr | I | 1 | CLK\_32M\_OK low or soft reset | Level(CLK\_32M domain) |
| FRAME\_DONE | I | 1 | A complete frame is received. | Level(CLK\_REG domain) |
| PROG\_LCTO | I | 3 | Long counter timeout program from COMM\_REG | Level(CLK\_REG domain) |
| PROG\_SCTO | I | 3 | Short counter timeout program from COMM\_REG | Level(CLK\_REG domain) |
| CLK\_32M\_OK | I | 1 | 1: CLK\_32M usable  0: CLK\_32M do not exit, or CLK\_32M is not accurate, or CLK\_32M will be off within 64us | async |
| SCAN\_MODE | I | 1 | Scan mode for DFT | level |

### Clock Domain

The clock for COMM\_TO is CLK\_REG\_SC.

### COMM\_TO function description

Pulse\_5ms is divided from pulse\_1M.

Cnt\_timeout[20:0] is defined to count for timeout time. It can be reset by rstb\_32M\_ok\_and\_sr low, or FRAME\_DONE high. The duration is listed in Table2.(HWR001\_COMM\_TO)

To count to expected time, the maximum number of cnt\_timeout is defined in Table2.

When cnt\_timeout reaches the max value defined by PROG\_SCTO, SET\_SCTO is high. (HWR002\_COMM\_TO)

When cnt\_timeout reaches the max value defined by PROG\_LCTO, SET\_LCTO and D2A\_LONG\_TO are high. (HWR003\_COMM\_TO)

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| PROG\_xCTO<2:0> | | | duration(ms) | cnt\_timeout max |
| 0 | 0 | 0 | 100 | 20 |
| 0 | 0 | 1 | 2000 | 400 |
| 0 | 1 | 0 | 10000 | 2000 |
| 0 | 1 | 1 | 60000 | 12000 |
| 1 | 0 | 0 | 180000 | 36000 |
| 1 | 0 | 1 | 600000 | 120000 |
| 1 | 1 | 0 | 1800000 | 360000 |
| 1 | 1 | 1 | 3600000 | 720000 |

Table2 maximum value of cnt\_timeout